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--32. A microcomputer according the claim 31, wherein the memory which stores a write control program is a mask ROM.

--33. A microcomputer according to claim 32, wherein the memory which stores a write control program is a RAM that receives the write control program from the ROM.

--34. A microcomputer according to claim 31, further comprising:

a data bus to which the central processing unit, the input and output unit, the ROM and the memory are coupled; and

an address bus to which the central processing unit, the input and output unit, the electrically programmable ROM and the memory are coupled.--

REMARKS

Applicants have canceled claims 21-30 without prejudice or disclaimer and have added new claims 31-34.

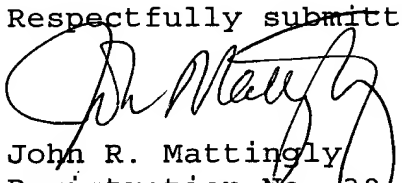
Claims 31-34 overcome the rejection under 35 U.S.C. § 102(b) as being anticipated by Ugon, U.S. Patent No. 4,382,279. In particular, claims 31 -34 are directed to a

microcomputer on a semiconductor chip that includes an electrically erasable and programmable ROM capable of storing a program and data, a memory in which a write control program for a writing to the ROM is stored and an input and output unit, wherein the central processing unit performs a writing to the ROM of the program or the data input from outside of the semiconductor chip via the input and output unit by controlling the write control circuit based on the write control program. Thus, the claimed combination is not anticipated or rendered obvious by the Ugon reference.

A Request for Continued Examination (RCE) is filed herewith to ensure entry of the newly added claims.

In view of the foregoing amendments and remarks, reconsideration and reexamination are respectfully requested.

Respectfully submitted,



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